**In the Claims:**

1. (Currently Amended) A processor for convolutional decoding, said processor embodying a pipelined superscalar processor core, comprising:

an instruction prefetch unit, the instruction prefetch unit configured to simultaneously fetch first and second Viterbi instructions and to partially decode and align the first and second Viterbi instructions;

an instruction sequencing unit, the instruction sequencing unit configured to fully decode the partially decoded first and second Viterbi instructions and to group the fully decoded first and second Viterbi instructions for simultaneous execution;

a first processing unit for executing a first Viterbi instruction, the instruction sequencing unit issuing the first Viterbi instruction to the first processing unit;

a second processing unit for executing a second Viterbi instruction, the instruction sequencing unit issuing the second Viterbi instruction to the second processing unit;

a register comprising a plurality of ordered bit positions; and

update logic coupled to the register, the first processing unit and the second processing unit, the update logic configured to receive a first signal indicative of a result of a first add-compare-select instruction from the first processing unit and a second signal indicative of a result of a second add-compare-select instruction from the second processing unit, the update logic further configured to update the contents of the register dependent upon the first and second signals;

wherein, in the event that: (1) the first signal but not the second signal, or (2) the second signal but not the first signal, is received, the update logic is configured to shift the contents of the register such that one bit position is vacated and to update the vacated bit position dependent on the received signal; and

wherein in the event the first and second signals are received substantially simultaneously, the update logic is configured to shift the contents of the register 2 bit positions in order thereby vacating 2 consecutive bit positions, to update one of the vacated bit positions dependent upon the first signal, and to update the other vacated bit position dependent upon the second signal.

2. (Original) The processor as recited in claim 1, wherein the first add-compare-select instruction and the second add-compare-select instruction each specify two add operations, a compare operation, and a select operation.

3. (Original) The processor as recited in claim 2, wherein the first add-compare-select instruction and the second add-compare-select instruction each specify a first pair of source operands and a second pair of source operands, and wherein each of the add operations specifies summing one of the first pair of source operands and one of the second pair of source operands.

4. (Original) The processor as recited in claim 2, wherein the compare operation comprises comparing results of the two add operations.

5. (Original) The processor as recited in claim 2, wherein the select operation comprises producing a result dependent upon a result of the compare operation.

6. (Previously Presented) The processor as recited in claim 2, wherein the processor is configured such that the first processing unit executes the first add-compare-select instruction and the second processing unit simultaneously executes the second add-compare-select instruction based upon a set of instruction grouping rules.

7-9: (Canceled)

10. (Currently Amended) A processor for decoding convolutional code, said processor embodying a pipelined superscalar processor core, comprising:

an instruction prefetch unit, said instruction prefetch unit configured to fetch at least two Viterbi instructions at a time and partially decode and align the at least two fetched Viterbi instructions;

an instruction sequencing unit, said instruction sequencing unit configured to group two of said at least two fetched Viterbi instructions for simultaneous execution;

an arithmetic logic unit (ALU);

a multiply/accumulate unit (MAU);

said instruction sequencing unit issuing a first one of the two Viterbi instructions to the ALU for execution thereby;

the instruction sequencing unit issuing a second one of the two Viterbi instructions to the MAU for execution thereby;

the ALU executing a first add-compare-select (ACS) operation on the first Viterbi instruction generally simultaneous with the MAU executing a second ACS operation on the second Viterbi instruction;

a register comprising a plurality of ordered bit positions; and

update logic coupled to the register, the ALU and the MAU, the update logic configured to receive the first signal issued by the ALU and the second signal issued by the MAU, the update logic updating the contents of the register based upon the first signal issued by the ALU and the second signal issued by the MAU;

wherein in the event that the first signal issued by the ALU and the second signal issued by the MAU are received substantially simultaneously, the update logic shifting the contents of the registry 2 bit positions in order to vacate 2 consecutive bit positions of the register, the update logic updating one of the vacated bit positions based upon the first signal issued by the ALU and updating the other vacated bit position based upon the second signal issued by the MAU.

11. (Original) The processor as recited in claim 10, wherein each of the two add-compare-select instructions specifies two add operations, a compare operation, and a select operation.

12. (Original) The processor as recited in claim 11, wherein each of the two add-compare-select instructions specifies a first pair of source operands and a second pair of source operands, and wherein each of the two add operations specifies summing one of the first pair of source operands and one of the second pair of source operands.

13. (Original) The processor as recited in claim 11, wherein the compare operation comprises comparing results of the two add operations.

14. (Original) The processor as recited in claim 11, wherein the select operation comprises producing a result dependent upon a result of the compare operation.

15. (Previously Presented) The processor as recited in claim 10, wherein the two add-compare-select instructions are dispatched to the ALU and the MAU for simultaneous execution dependent upon a set of instruction grouping rules.

16-22: (Canceled)

23. (New) The processor as recited in claim 1 and further comprising an execution unit, the first and second processing units residing within the execution unit.

24. (New) The processor as recited in claim 1, wherein the instruction prefetch unit further comprises an instruction cache in which the partially decoded and aligned instructions are stored.

25. (New) The processor as recited in claim 10, and further comprising an execution unit, the ALU and the MAU residing within the execution unit.

26. (New) The processor as recited in claim 10, wherein the instruction prefetch unit further comprises an instruction cache in which the partially decoded and aligned instructions are stored.